Integrated Solutions for TSMC InFO Designs

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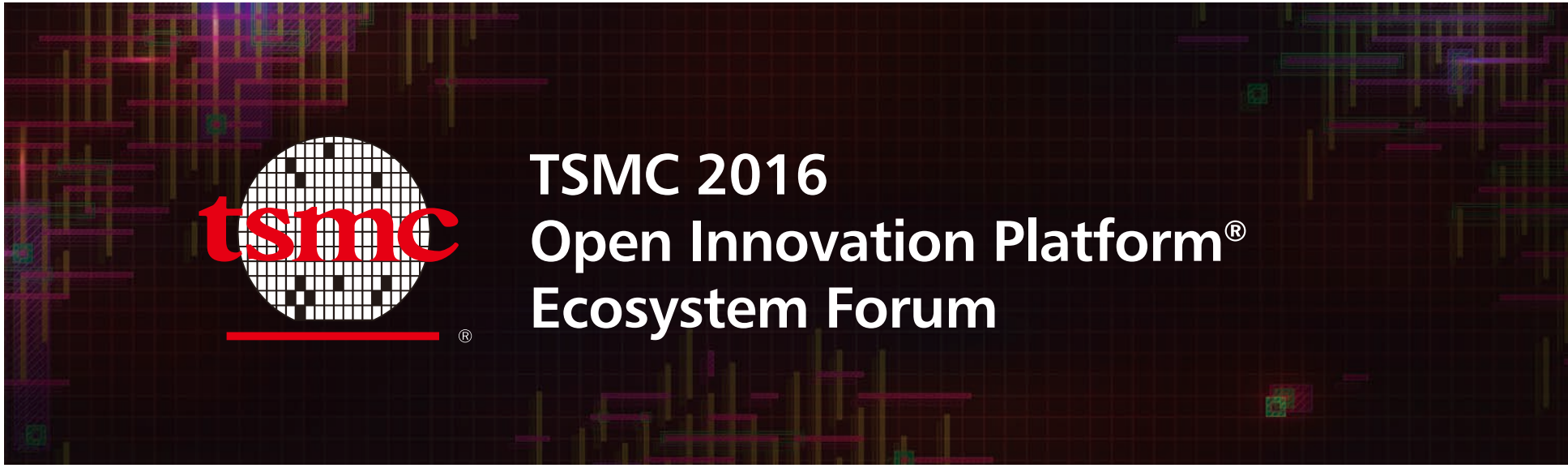

ABSTRACT

TSMC's InFO advanced wafer-level packaging technology provides cost-effective system scaling to increase system bandwidth, and enables heterogeneous integration for smaller power consumption, and smaller form factor. Designers need to do much tighter co-design among multi-die and package, as well as more concurrent sign off and co-analysis across physical, electrical, and thermal aspects, in order to take advantage of the InFO technology.

Cadence's newly developed methodology provides a holistic solution to cover the entire implementations and verifications of the heterogeneous design, a platform that provides seamlessly integrated flow across digital SOC, custom IC, and InFO packaging tools, from collaboirative work with TSMC, as well as a key strategic customer.

This paper will present the highlights of above platform, and then details the key enabling features of tools involved. It will also give examples of how to deploy the methodologies for various applications using TSMC InFO technologies, including large SOC multi-die InFO designs, as well as RF/Analog centric InFO PoP system.

The presentation starts with InFO design and layout platform, with enhanced features such as vectorization, In-Design Design rule checking, and IC-level physical sign off accuracy; it then covers the methodology of electrical-migration, IR drop analysis, and layer-based thermal analysis concurrently among multi-dies and InFO package with cross probing capabilities. The paper also provide an enhanced electro-magnetic interference analysis to showcase InFO's advantageous material property for RF design.

At the end, the presentation illustrates multiple extraction solutions tailored for various application of InFO, including a RC parasitic generation for cross-die static timing analysis, RLCK equivalent model for signal integration analysis in time domains, as well as S-parameter extraction for power integrity for InFO based package.

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TSMC OIP Ecosystem Forum
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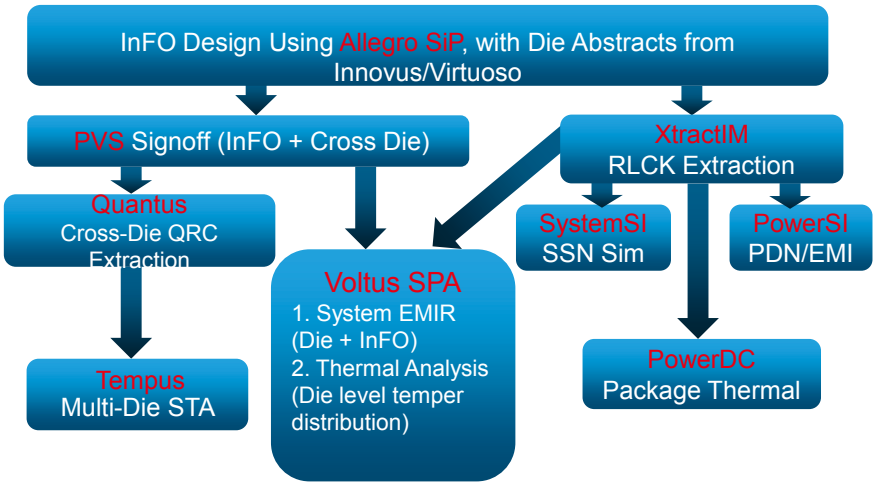
InFO Design and Analysis Integrated Flow Overview



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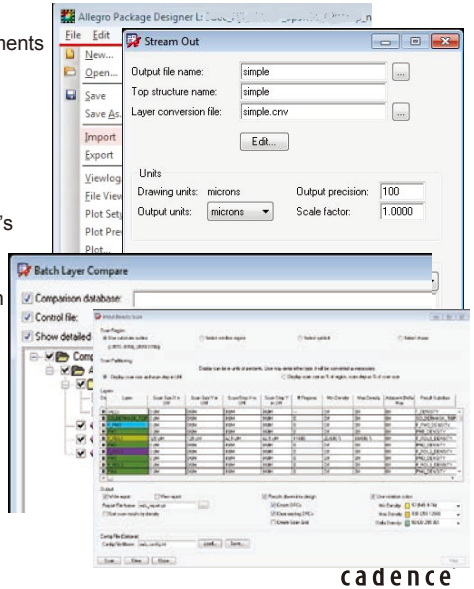
Designated InFO Features Built in Allegro SiP

- Supports specific manufacturing requirements of InFO
  - Focus on very thin and balanced metal–minimizing warpage
  - Focus on localized metal density; meshed metal, meshed pads
- Layer compare—allow InFO designer to compare GDS to layout local to the tool (without a CAM tool), used as a designer's check prior to sending artwork to TSMC
- Speed/automation/fast turnaround, with iPVS integrated, to support in-design DRC check, with IC-level signoff quality
- Intelligent stream outputs, including vectorized GDS2, Verilog, and CDL formats to work seamlessly with IC tools
- Supports InFO-S and InFO_PoP designs
- Fast, efficient routing; leverage pin optimization if available



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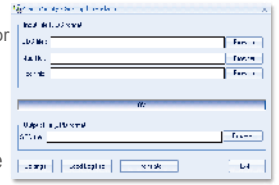
SoC DB (GDS2) and InFO SiP DB Merge Utility for Integrated SI, PI, and EMI Analysis

- SoC
  - Input from die DBs:
    - Hierarchy structure of gds for metal and via layers
    - Gds layer mapping file
    - Label text gds for net naming
    - Die pin test file: pin name, XY-coordinate, and net name
    - Cell structure name for bump pad generates a circuit component connecting with InFO
  - Output:
    - Translate gds into spd by Cadence® Sigrity™ Gds2Spd translator
      - SoC die flipped
      - Via cut is transferred to pad-stack
- InFO
  - Input: Cadence SiP Layout design
  - Directly import into Sigrity solution, saved-as spd file
- Merged DB is ready for Sigrity analysis
  - InFO spd as base, merge SoC spd directly in Sigrity



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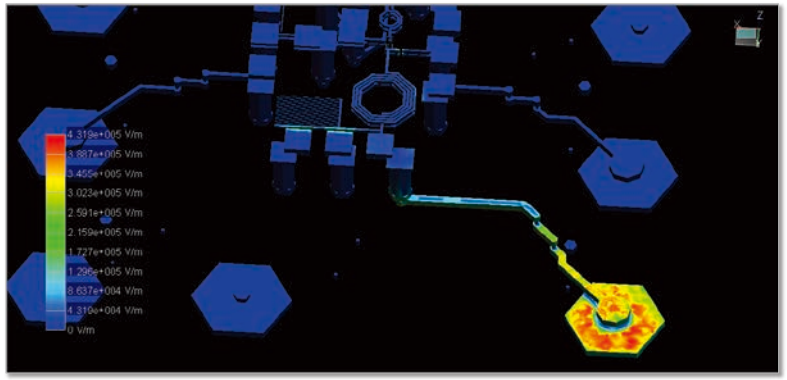
Electro-Magnetic Interference (EMI) in Sigrity PowerSI 3DEM

- SoC + InFO package



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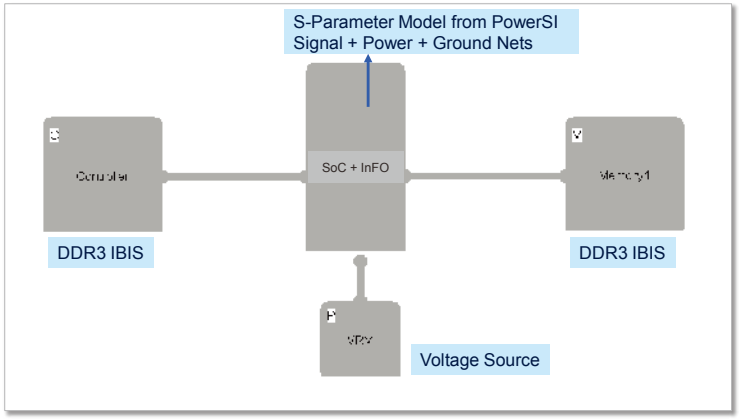
SSN Block Diagram in Sigrity SystemSI



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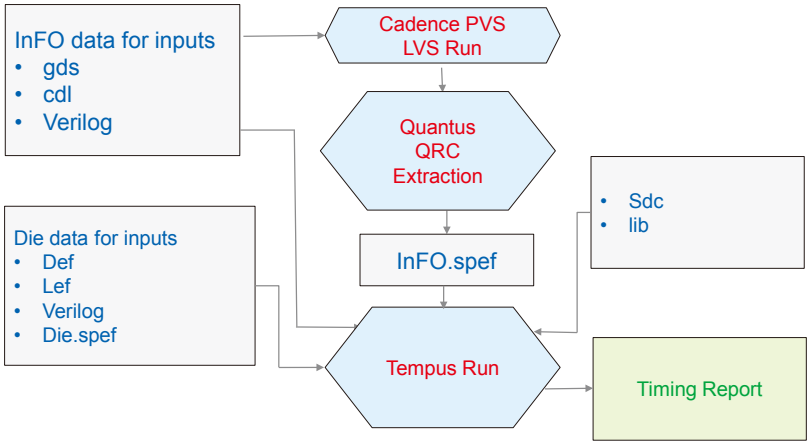
InFO Cross Die Tempus STA Flow



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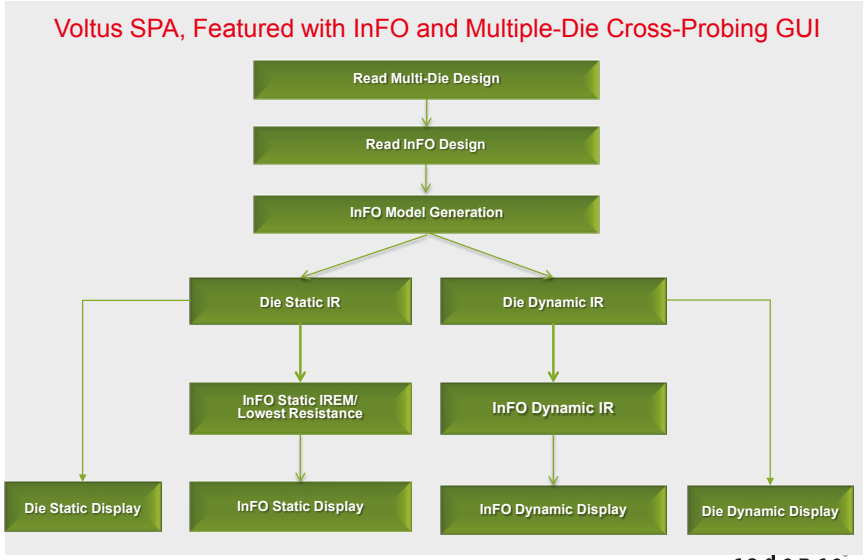
Voltus SPA Co-Simulation Flow for Concurrent EMIR



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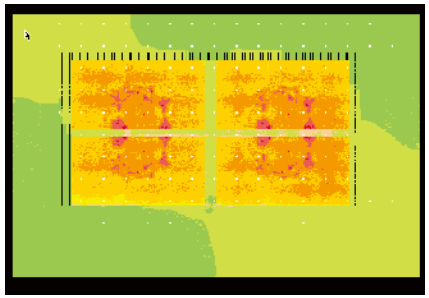
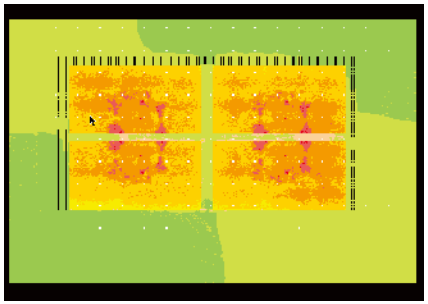
Die Static IR Result

VDD_chip1 : ir



VDD_chip2 : ir



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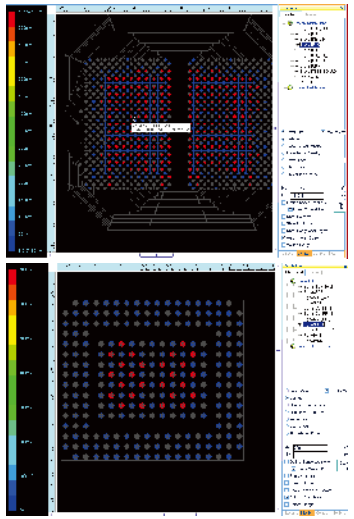
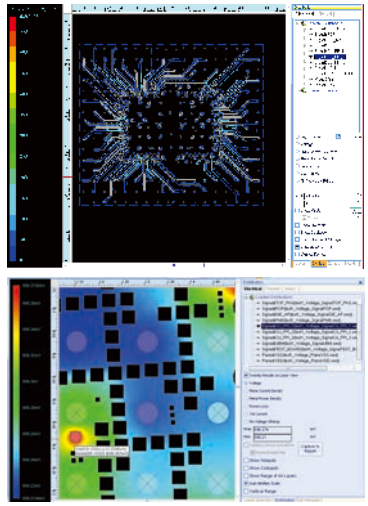
InFO Static Voltage Result Display





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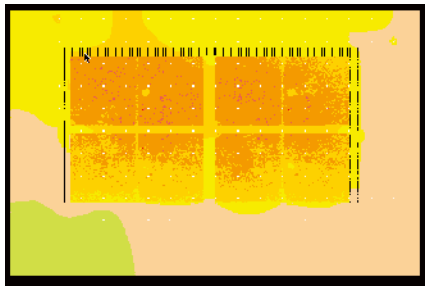
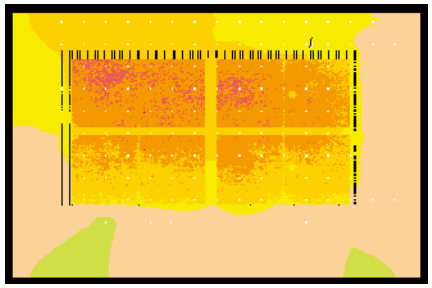
Die Dynamic IR Result

VDD_chip1 : ir



VDD_chip2 : ir



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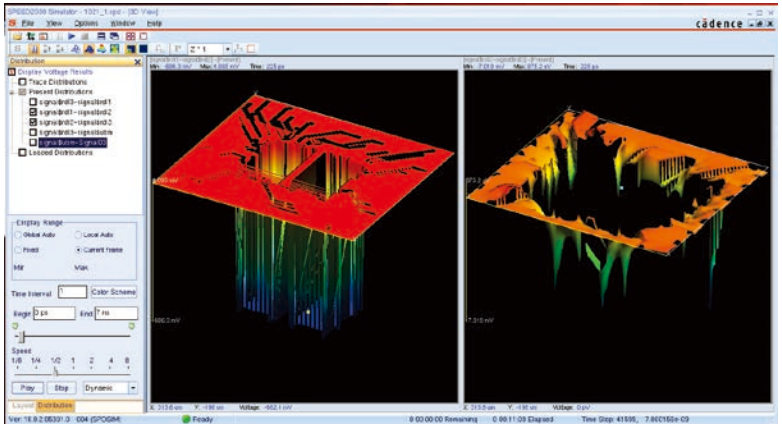
InFO Dynamic IR Results

Snapshot of voltage movie



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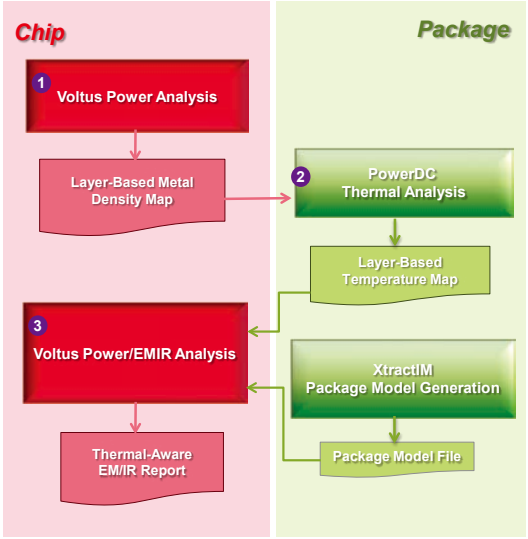
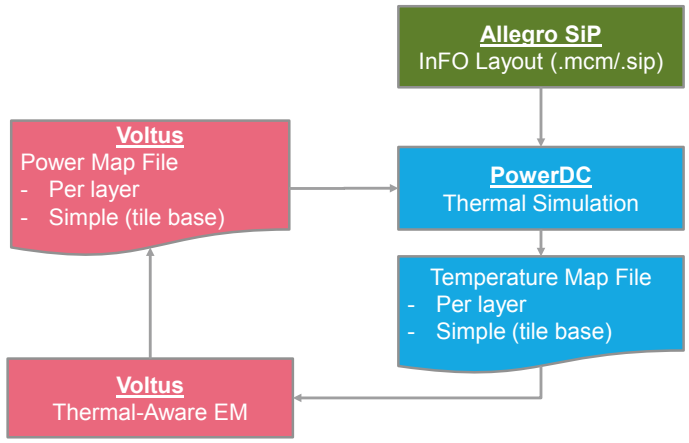
Voltus IC/Pkg Thermal-Aware EM Flow



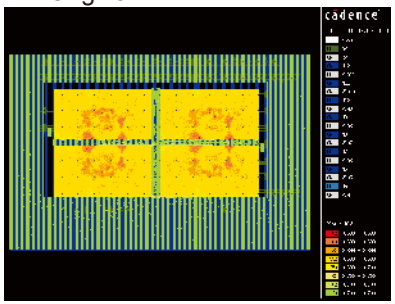
1. Cadence Voltus™ IC Power Integrity Solution runs power analysis to generate layer-based metal density map
2. Cadence Sigrity PowerDC™ technology gets the input file and generates a layer-based temperature map
3. Voltus solution re-runs power and EMIR with given new layer-based temperature

Sigrity PowerDC Thermal Flow for Voltus Thermal-Aware EM Simulation

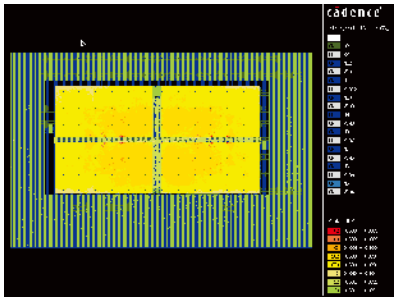


Voltus IR Comparison with/without Thermal Map

- Original IR



- Thermal-Aware IR



Conclusions

- Cadence Allegro® SiP provides natively built features for InFO
  - In-design DRC, flexible output DB format, and high-performance optimization
- Cadence PVS provides cross-die LVS/DRC, including all special design rules from InFO
  - With iPVS embedded in Allegro SiP, signoff results will be always in sync with implantation
- Merged DB (InFO and die) for SI, PI, EMI analysis for the integrated InFO system
  - Allows system-level analysis of cross-coupling between InFO and multiple dies
- Voltus SPA integrated with Sigrity engines for InFO system-level concurrent EMIR
  - Now with one-button batch mode and cross-probing GUI mode
- Cadence Quantus™ QRC Extraction Solution for cross-die/InFO static timing analysis
  - A true distributed SPEF instead of lumped SPEF of InFO for accurate cross-die timing analysis
- Integrated flow validated in both multi-die digital SoC + InFO and Aaalog/RD die + InFO

NOTE